

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (Currently amended) A method to facilitate cache coherence with
2 adaptive write updates, comprising:
3 | initializing a cache to operate using a write-invalidate protocol, wherein
4 | this initializing is performed by a cache controller residing in a processor;
5 | monitoring a dynamic behavior of the cache during program execution,
6 | wherein monitoring the dynamic behavior of the cache involves maintaining a
7 | count for each cache line of the number of cache line invalidations the cache line
8 | has been subject to during program execution, wherein this monitoring is
9 | performed by the cache controller in the processor; and
10 | if the dynamic behavior indicates that better performance can be achieved
11 | using a write-broadcast protocol, switching the cache to operate using the write-
12 | broadcast protocol, wherein this switching is performed by the cache controller in
13 | the processor.

1 2 (Canceled).

1 | 3. (Currently amended) The method of ~~claim 2~~ claim 1, wherein switching
2 | to the write-broadcast protocol involves switching to the write-broadcast protocol
3 | on a cache-line by cache-line basis.

1 4 (Canceled).

1 5. (Previously presented) The method of claim 1, wherein if the number of
2 cache line invalidations indicates that a given cache line is updated frequently,
3 switching the cache line to operate under the write-broadcast protocol.

1 6. (Original) The method of claim 5, wherein if a given cache line is using
2 the write-broadcast protocol and the number of cache line updates indicates that
3 the given cache line is not being contended for by multiple processors, switching
4 the given cache line back to the write-invalidate protocol.

1 7. (Currently amended) The method of claim 1, wherein if a shared
2 memory multiprocessor includes ~~modules~~ caches that are not able to switch to the
3 write-broadcast protocol, the method further comprises locking the cache into the
4 write-invalidate protocol.

1 8. (Currently amended) The method of claim 1, wherein when a cache is
2 operating under the write-invalidate protocol, sends an invalidation message is
3 sent to other caches in a shared memory multiprocessor when a given cache line is
4 updated in a local cache.

1 9. (Currently amended) The method of claim 1, wherein when a cache is
2 operating under the write-broadcast protocol, broadcasts an update is broadcast to
3 other caches in a shared memory multiprocessor when the given cache line is
4 updated in a local cache.

1 10. (Currently amended) An apparatus to facilitate cache coherence with
2 adaptive write updates, comprising:

3 an initializing mechanism configured to initialize a cache to a write-
4 invalidate protocol, wherein the initializing mechanism is present in a cache
5 controller in a processor;
6 an monitoring mechanism configured to monitor a dynamic behavior of
7 the cache, wherein monitoring the dynamic behavior of the cache involves
8 maintaining a count of cache line invalidations initiated by each processor within
9 a shared memory multiprocessor, wherein the monitoring mechanism is present in
10 the cache controller in the processor; and
11 a protocol switching mechanism configured to switch the cache to a write-
12 broadcast protocol if the dynamic behavior indicates that better performance can
13 be achieved using the write-broadcast protocol, wherein the protocol switching
14 mechanism is present in the cache controller in the processor.

1 11 (Canceled).

1 12. (Currently amended) The apparatus of ~~claim 11~~ claim 10, wherein
2 switching to the write-broadcast protocol involves switching to the write-
3 broadcast protocol on a cache-line by cache-line basis.

1 13 (Canceled).

1 14. (Previously presented) The apparatus of claim 10, wherein if the count
2 of cache line invalidations indicates that a given cache line is updated frequently
3 in different caches of the shared memory multiprocessor, switching the cache to
4 the write-broadcast protocol.

1 15. (Original) The apparatus of claim 14, wherein if the given cache line is
2 using the write-broadcast protocol and the count of cache line invalidations

3 indicates that the given cache line is being invalidated in only one cache,
4 switching the cache to the write-invalidate protocol.

1 16. (Currently amended) The apparatus of claim 10, further comprising a
2 locking mechanism configured to lock the cache into the write-invalidate protocol
3 if the shared memory multiprocessor includes ~~modules~~ caches that are not able to
4 switch to the write-broadcast protocol.

1 17. (Currently amended) The apparatus of claim 10, wherein when the
2 cache is operating under the write-invalidate protocol, ~~involves sending an~~
3 invalidate message is sent to other caches within a shared memory multiprocessor
4 when a given cache is written to.

1 18. (Currently amended) The apparatus of claim 10, wherein when the
2 cache is operating under the write-broadcast protocol, ~~involves broadcasting a~~
3 data update message is broadcast to other caches within a shared memory
4 multiprocessor when a given cache is written to.

1 19. (Currently amended) A computing system that facilitates cache
2 coherence with adaptive write updates, comprising:
3 a plurality of processors, wherein a processor within the plurality of
4 processors includes a cache;
5 a shared memory;
6 a bus coupled between the plurality of processors and the shared memory,
7 wherein the bus transports addresses and data between the shared memory and the
8 plurality of processors

9 an initializing mechanism configured to initialize the cache to a write-
10 invalidate protocol, wherein the initializing mechanism is present in a cache
11 controller in a processor;
12 a monitoring mechanism configured to monitor a dynamic behavior of the
13 cache, wherein monitoring the dynamic behavior of the cache involves
14 maintaining a count of cache line invalidations initiated by each processor within
15 a shared memory multiprocessor, wherein the monitoring mechanism is present in
16 the cache controller in the processor; and
17 a protocol switching mechanism configured to switch the cache to a write-
18 broadcast protocol if the dynamic behavior indicates that better performance can
19 be achieved using the write-broadcast protocol, wherein the protocol switching
20 mechanism is present in the cache controller in the processor.

1 20. (Currently amended) A means to facilitate cache coherence with
2 adaptive write updates, comprising:
3 an initializing means for initializing a cache to a write-invalidate protocol,
4 wherein the initializing means is present in a cache controller in a processor;
5 a monitoring means for monitoring a dynamic behavior of the cache,
6 wherein monitoring the dynamic behavior of the cache involves monitoring the
7 dynamic behavior of the cache on a cache-line by cache-line basis, wherein the
8 monitoring means is present in the cache controller in the processor; and
9 a protocol switching means for switching the cache to a write-broadcast
10 protocol if the dynamic behavior indicates that better performance can be
11 achieved using the write-broadcast protocol, wherein the protocol switching
12 means is present in the cache controller in the processor.